ABSTRACT

A chip carrier for testing electrical performance of a passive component includes: a core layer having a plurality of conductive traces on a surface thereof; at least one first trace connected with the passive component and having a first predetermined position and two ends, wherein the two ends are respectively electrically connected to a first bond finger on the surface of the chip carrier and to a first ball pad on an opposite surface of the chip carrier; at least one second trace not connected with the passive component and having two ends and a second predetermined position located on the same surface as the first predetermined position, one end of the second trace being electrically connected to a second ball pad located on the same surface as the first ball pad; and a solder mask layer applied over the conductive traces, with the first and second predetermined positions exposed.

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